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H3P PHD
H3T T2T3F T4D T5E

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# (54) Interface circuits

(57) A double voltage source interface circuit comprises an n channel CMOS transistor ($n_1$) coupled to the output of the circuit by way of a latch circuit (1). The input signal is also coupled to the output by way of an inverter ($IV_a$) and a further n channel transistor ($n_2$). A high level source ($V_H$) is applied to the latch circuit (1), whereas a low level voltage source ($V_L$) is connected to the inverter ($IV_a$). The circuit is able to produce an output switching between a low level and the high level of the voltage source ($V_H$) in response to an input which changes from low level to the lower high level of the voltage source ($V_L$) without an unnecessary dissipation of power. The inverter $IV_a$ may be of the type shown at $IV_1$; $IV_2$ in figure 1 (not shown). Depending on whether $n_1$ or $n_2$ conducts in response to input level, the level at P or Q is inverted by $IV_a$ or $IV_b$. Spurious conduction affecting output level or state is avoided.

FIG.3

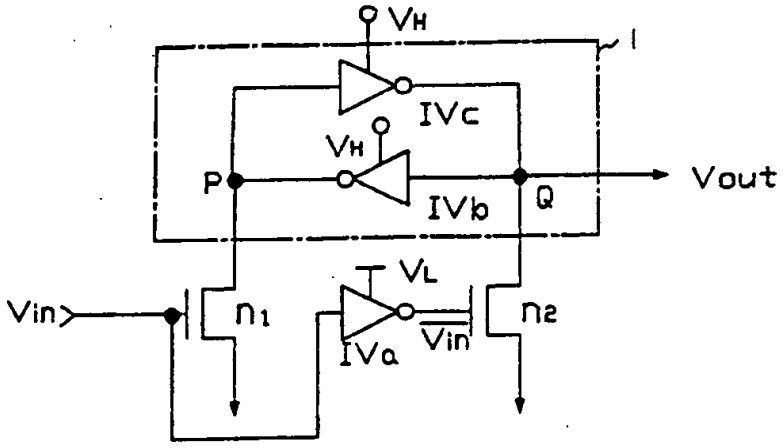


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FIG.1
(PRIOR ART)

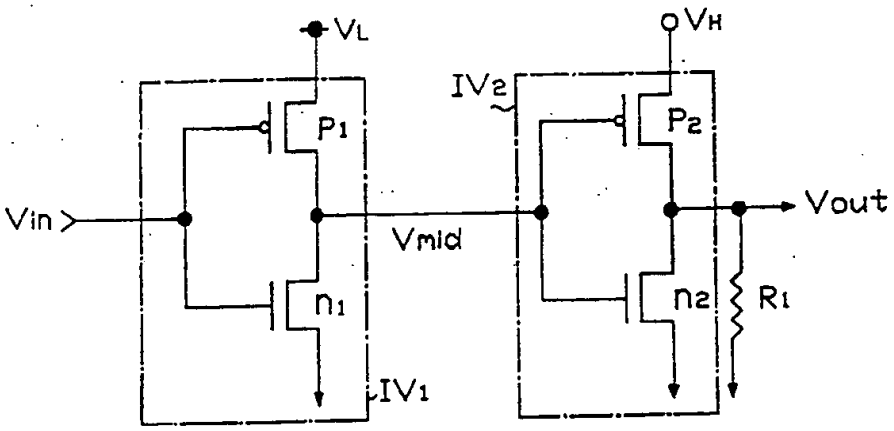



FIG.2

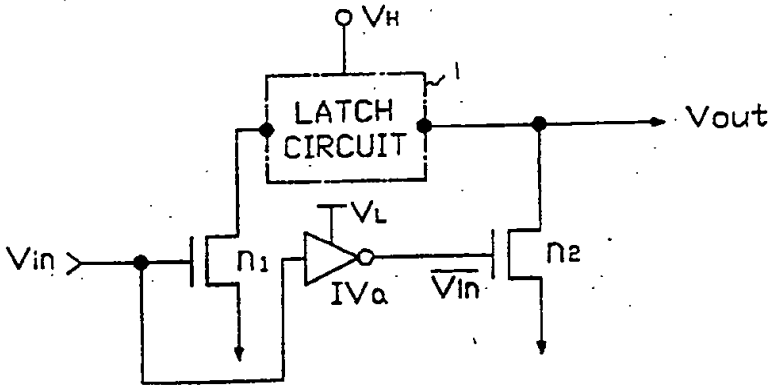



FIG.3

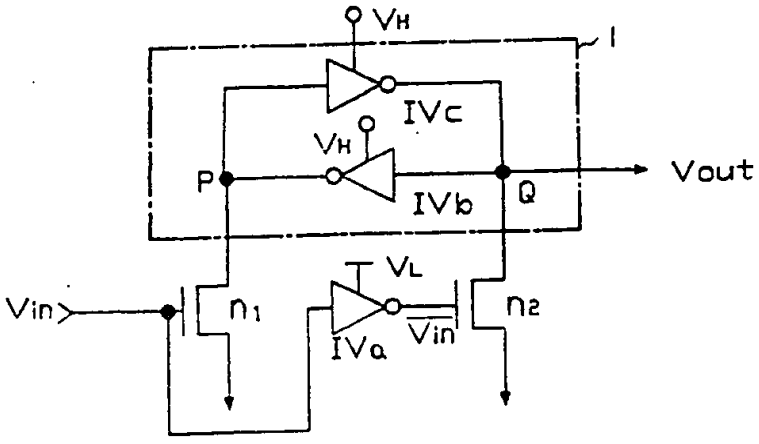


FIG.4A

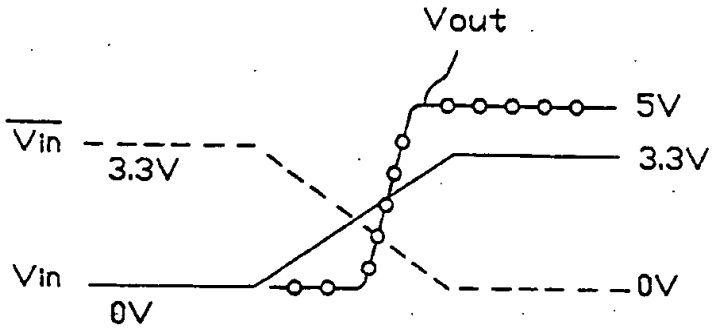
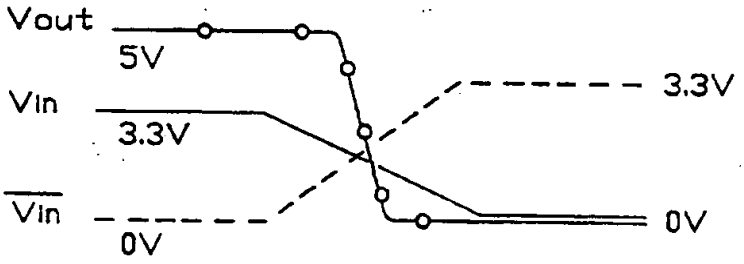

Vout
5V
3.3V
0V
$\overline{Vin}$
3.3V
Vin
0V

FIG.4B


Vout
5V
Vin
3.3V
$\overline{Vin}$
0V
3.3V
0V

# A DOUBLE VOLTAGE SOURCE INTERFACE CIRCUIT

The present invention relates to a double voltage source interface circuit.

A double voltage source interface circuit is used, for example, for driving a circuit requiring a high voltage from a source of low voltage in a chip having two kinds of power voltage, for example a low voltage and a high voltage.

A conventional double voltage source interface circuit comprises two inverters, one of which is powered by the low voltage source, and the other of which is powered from the high voltage source. However, with such an arrangement the second inverter may be found to draw power when it should be turned off whereby the overall consumption of power of the circuit is increased. In addition, the output of the second inverter can be turned on, when it ought to be off, thereby providing errors.

The present invention seeks to provide a double voltage source interface circuit in which the disadvantages of the prior art circuits are reduced.

According to the present invention there is provided a double voltage source interface circuit comprising a first inverter coupling an input to an output, and a second inverter coupling the input to the output, and further comprising latching means coupling said first inverter to the output, and wherein said latching means is arranged to be connected to a first voltage source, and said second inverter is arranged to be coupled to a second voltage source.

Preferably, said first inverter comprises a field

effect transistor whose gate is connected to the input and whose drain-source path is connected to said latching means.

In an embodiment, said second inverter is connected directly to said input and is coupled to said output by way of a third inverter. For example, the third inverter may comprise a field effect transistor.

In a preferred embodiment said first inverter is a first n channel CMOS transistor whose gate is connected to the input and whose drain source path is connected to said latching means, and wherein said latching means is arranged to be connected to a high level voltage source. Said second inverter may be connected directly to said input and is arranged to be connected to a low level voltage source. In this case, the output of said second inverter is preferably connected to the gate of a second n channel CMOS transistor.

For example, said latching means is connected to the drains of said first and second n channel CMOS transistors.

In an embodiment, said latching means comprises two inverters connected in parallel.

The invention also extends to a double voltage source interface circuit comprising n channel CMOS transistor for inputting an input signal to its gate; an inverter for converting the input signal; and a n channel CMOS transistor for inputting the output from the inverter to its gate, wherein a latch circuit having a high voltage source is connected between the drains of the CMOS transistors.

Preferably, the latch circuit is comprised of two

inverters.

Embodiments of the present invention will hereinafter be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 shows the circuit diagram of a known double voltage source interface circuit,

Figure 2 shows a general block diagram of a double voltage source interface circuit of the present invention,

Figure 3 shows schematically a circuit diagram of the circuit of Figure 2, and

Figures 4A and 4B show the input and output voltages generated at parts of the double voltage source interface circuit as shown in Figures 2 and 3.

Figure 1 shows an example of a conventional double voltage source interface circuit connected to two power sources $V_L$ and $V_H$. The interface circuit comprises a first inverter $IV_1$ and a second inverter $IV_2$. The first inverter $IV_1$ comprises a p channel CMOS field effect transistor $p_1$ whose drain is connected to the voltage source $V_L$. The drain-source path of the transistor $p_1$ is connected to the drain-source path of a n channel CMOS transistor $n_1$. The gates of the transistors $p_1$ and $n_1$ are connected to an input to receive an input voltage Vin. The output voltage Vmid of the inverter $IV_1$ is taken at the connection of the drain source paths of the two transistors $p_1$ and $n_1$ and is applied to the gates of similarly arranged p and n channel transistors $p_2$ and $n_2$ forming the second inverter $IV_2$. It will be seen that the drain of the p channel transistor $p_2$ is connected to a high level voltage source $V_H$. The output of the interface circuit is taken from the connection

between the transistors $p_2$ and $n_1$ and it will be seen that a resistor $R_1$ forming a current path is connected to the output.

Let us assume that the input voltage Vin changes between a low level of approximately 0V and a high level of approximately 3.3V. Let us also assume that the voltage of the source $V_L$ is of the order of 3.3V, whereas the voltage of the high level source $V_H$ is about 5V.

It will be appreciated that as the voltage Vin applied to the first inverter $IV_1$ swings between its high and low levels, the output Vmid of the inverter swings correspondingly and also has a low level of about 0V and a high level of approximately 3.3V. This voltage output is applied as an input to the inverter $IV_2$. However, because of the level of the voltage of the source $V_H$, when the input Vmid to the inverter $IV_2$ changes between the values of 0V and 3.3V, the output of the inverter $IV_2$, which is Vout, swings between 0V and 5V.

It will be appreciated that both of the inverters $IV_1$ and $IV_2$ operate in the same manner. Thus, when the input voltage is at a low level the n channel transistor $n_1$ or $n_2$ is turned off and the p channel transistor $p_1$ or $p_2$ is turned on pulling the ouput Vmid or Vout to the voltage level of the voltage source $V_L$ or $V_H$. When the input signal voltage goes high, the p channel transistors $p_1$ or $p_2$ are turned off in their turn, the n channel transistors $n_1$ or $n_2$ conduct, and the respective output Vmid or Vout is pulled to the low level, for example, to ground. When the output of the first inverter $IV_1$ is at 0V such that the p channel transistor $p_2$ is turned on, a current path through the p channel transistor $p_2$ and the resistor $R_1$ is formed. The voltage on the ouput Vout is at the high level 5V. When the output of the first inverter $IV_1$ is high, that is

at 3.3V, the p channel transistor $p_2$ is turned off, and the n channel transistor $n_2$ is turned on such that the output Vout is low, that is at 0V. However, in this case, there is a gate drain voltage across the p channel transistor $p_2$ of approximately 1.7V (5V - 3.3V = 1.7V) and this may be sufficient to turn on the transistor $p_2$ so that current flows by way of the transistor $p_2$ through the resistor $R_1$. In this case, the consumption of power is increased because there is a current flow when such would not normally be expected. If the resistor $R_1$ is not provided, so that there is no current path, the transistor $p_2$ may be fully turned on such that the output voltage Vout becomes high and thereby gives an erroneous output.

Figure 2 shows a general block diagram of a double voltage source interface circuit of the present invention which avoids the problems described above with reference to Figure 1. Figure 3 is a schematic circuit diagram of the circuit of Figure 2 and in particular shows the construction of the latch circuit. The operation of the circuit shown in Figures 2 and 3 will be better understood by reference to Figures 4A and 4B showing input and output wave forms generated by the circuit of the invention.

It will be seen from Figure 2 that the circuit of the invention comprises an input to which the input voltage Vin is applied. First and second inverters $n_1$ and $IV_a$ are connected to this input. As can be seen, the first inverter is in the form of an n channel CMOS transistor $n_1$ having its gate arranged to receive the input Vin and its drain source path connected to a latch circuit 1. The second inverter $IV_a$ is also connected directly to the input to receive the input signal Vin. The second inverter $IV_a$ may be constructed by any suitable means, but is preferably an inverter of the same type as $IV_1$ and $IV_2$ of Figure 1. It will be seen that the low voltage source $V_L$ is connected

to the second inverter $IV_a$ whereas the high voltage source $V_H$ is connected to the latch circuit 1. The output of the latch circuit 1 is connected to the output of the interface circuit at which the voltage Vout appears. The output of the second inverter $IV_a$ is coupled to the output of the circuit by way of a third inverter $n_2$. In the embodiment illustrated this third inverter is a n channel CMOS transistor $n_2$ having its gate connected to the output of the inverter $IV_a$ and its drain source path connected to the output of the interface circuit.

We shall consider again that the high and low voltage levels for the circuit of Figure 2 are the same as described above with reference to Figure 1. Thus, the low level is approximately 0V whereas the high level is either 3.3V, if it emanates from the voltage source $V_L$, or 5V if supplied from the voltage source $V_H$. The input signal Vin can swing between low level and high level, that is between 0V and 3.3V, and is applied to the gate of the transistor $n_1$ such that the transistor $n_1$ is turned off when Vin is low and turned on when Vin is high. Vin is also applied to the inverter $IV_a$ such that $\overline{Vin}$ is output and applied to the gate of the transistor $n_2$. It will therefore immediately be appreciated that when transistor $n_1$ is turned on, transistor $n_2$ is turned off, and vice versa.

It can be seen from Figure 3 that the latch circuit 1 comprises two inverters $IV_b$ and $IV_c$, connected in parallel between nodes P and Q and each connected to the high level voltage source $V_H$. When the input signal Vin changes between a low level and a high level signal, that is between 0V and 3.3V, the output signal from node Q of the latch 1 changes between 0V and 5V as is indicated in Figures 4A and 4B. Thus, if Vin goes high such that the transistor $n_1$ is switched on, the node P goes low and the inverter $IV_c$ applies the voltage level of source $V_H$ to node

Q which thereby goes high. At the same time transistor $n_2$ is turned off such that the high level voltage $V_H$ at the node Q is the output Vout.

Similarly, when the input voltage Vin goes low such that transistor $n_1$ is switched off, transistor $n_2$ is turned on to put a low level signal on the input to inverter $IV_b$ and also to connect Vout to the low level so that Vout also goes low. At this time the node Q will be at 0V and thus the inverter $IV_b$ connects the voltage level of the source $V_H$ to the node P which will thus be at 5V. If then the input signal Vin goes high, so that the transistor $n_1$ is turned on and the transistor $n_2$ is turned off, the transistor $n_1$ can conduct and thereby pull the node P down to 0V. However, it will be appreciated that the current path through $N_1$ is isolated from the output Vout which is switched to the 5V high level.

With the input signal high and Vout similarly high, node Q will be at 5V and node P will be at 0V. If Vin then goes low, switching off transistor $n_1$ and turning on transistor $n_2$, a current path for the voltage at node Q is formed through the transistor $n_2$ so that the potential of node Q is maintained at 0V.

It will be appreciated that the circuit of Figures 2 and 3 acurately brings the voltage at the output of the circuit to the level required, but that there is no current path for dissipating voltage from the high level source $V_H$ as with the prior art. Accordingly, the unnecessary dissipation of power is reduced.

It will be appreciated that modifications to and developments of the present invention as described and illustrated may be made within the scope of the claims.

CLAIMS

1. A double voltage source interface circuit comprising a first inverter coupling an input to an output, and a second inverter coupling the input to the output, and further comprising latching means coupling said first inverter to the output, and wherein said latching means is arranged to be connected to a first voltage source, and said second inverter is arranged to be coupled to a second voltage source.

2. A double voltage source interface circuit as claimed in Claim 1, wherein said first inverter comprises a field effect transistor whose gate is connected to the input and whose drain-source path is connected to said latching means.

3. A double voltage source interface circuit as claimed in Claim 1 or 2, wherein said second inverter is connected directly to said input and is coupled to said output by way of a third inverter.

4. A double voltage source interface circuit as claimed in Claim 3, wherein said third inverter comprises a field effect transistor.

5. A double voltage source interface circuit as claimed in any preceding claim, wherein said first inverter is a first n channel CMOS transistor whose gate is connected to the input and whose drain source path is connected to said latching means, and wherein said latching means is arranged to be connected to a high level voltage source.

6. A double voltage source interface circuit as claimed in Claim 5, wherein said second inverter is connected directly to said input and is arranged to be connected to a

low level voltage source.

7. A double voltage source interface circuit as claimed in Claim 6, wherein the output of said second inverter is connected to the gate of a second n channel CMOS transistor.

8. A double voltage source interface circuit as claimed in Claim 7, wherein said latching means is connected to the drains of said first and second n channel CMOS transistors.

9. A double voltage source interface circuit as claimed in any preceding claim, wherein said latching means comprises two inverters connected in parallel.

10. A double voltage source interface circuit comprising n channel CMOS transistor for inputting an input signal to its gate; an inverter for converting the input signal; and a n channel CMOS transistor for inputting the output from the inverter to its gate, wherein a latch circuit having a high voltage source is connected between the drains of the CMOS transistors.

11. A double voltage source interface circuit as claimed in Claim 10, wherein the latch circuit is comprised of two inverters.

12. A double voltage source interface circuit substantially as hereinbefore described with reference to the accompanying drawings.

**Patents Act 1977**
**Examiner's report to the Comptroller under Section 17 (The Search Report)**

Application number

9027194.1

**Relevant Technical fields**

(i) UK Cl (Edition K) H3P PHD

(ii) Int Cl (Edition 5) H03K

Search Examiner

MR S SATKURUNATH

**Databases** (see over)

(i) UK Patent Office

(ii)

Date of Search

28 February 1991

Documents considered relevant following a search in respect of claims

1-11

| Category (see over) | Identity of document and relevant passages | Relevant to claim(s) |
|---|---|---|
| X | GB 2 103 897 (MITEL) | 1,10 |
| X | EP 0 220 833 (KABUSHIKI) | 1,10 |

G06ABH

SF2(p)

| Category | Identity of document and relevant passages | Relevant to claim(s) |
|---|---|---|
| | | |

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